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Engineering Note

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Project: CFT Axial
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Subject: Clock Control Notes for CFT Front End Cards

Introduction

This note describes the clock generation logic for the MCM Test Board, which will also be used on the CFT front end cards. The interfaces from the clock generation logic to the SVX Sequencer, the VME Test Beam Generator (VTBG) and the on-board microcontroller are re-examined.

System Timing Structure

Both the MCM Test Board and the CFT Front End boards have two modes of operation:

- Internal Clock Mode, in which no connection to the SVX Sequencer is present, and
- External Clock Mode, in which an SVX Sequencer is present and it is the source of clocks.

External Clock Mode

In External Mode, the SVX Sequencer provides a Crossing Clock (XING) which is a pulse of approximately 20 nsec duration that occurs every 132 nsec. Two clock qualifiers are provided. The SYNC_GAP signal indicates that the accelerator is not providing collisions and maintenance functions may be performed. The FIRST_CROSSING signal indicates that the XING edge is the first one associated with accelerator data after a SYNC_GAP.

The general response of the clock system in External Mode is to enter a SIFT reset cycle upon the receipt of SYNC_GAP, and after the reset cycle is complete, wait for FIRST_CROSSING before re-enabling the various SIFT clocks for acquisition mode. The clock generator drives the PRST, DRST, S/H and READ clocks to the SIFT in one of two cycles, the Acquisition Cycle and the Reset Cycle. Timing for the Acquisition Cycle is based upon the edge of the XING clock and is controlled by delay lines. Timing for the Reset Cycle is controlled by the local 53 MHz oscillator. Figure 1 shows normal Acquisition Mode timing; figure 2 shows the Reset Cycle.

Fine timing is generated by a multiple tap delay line which creates copies of XING delayed from 5 nsec to 150 nsec in 5 nsec steps. Other timing is available from an approximate 53 MHz signal derived from the XING delay taps.

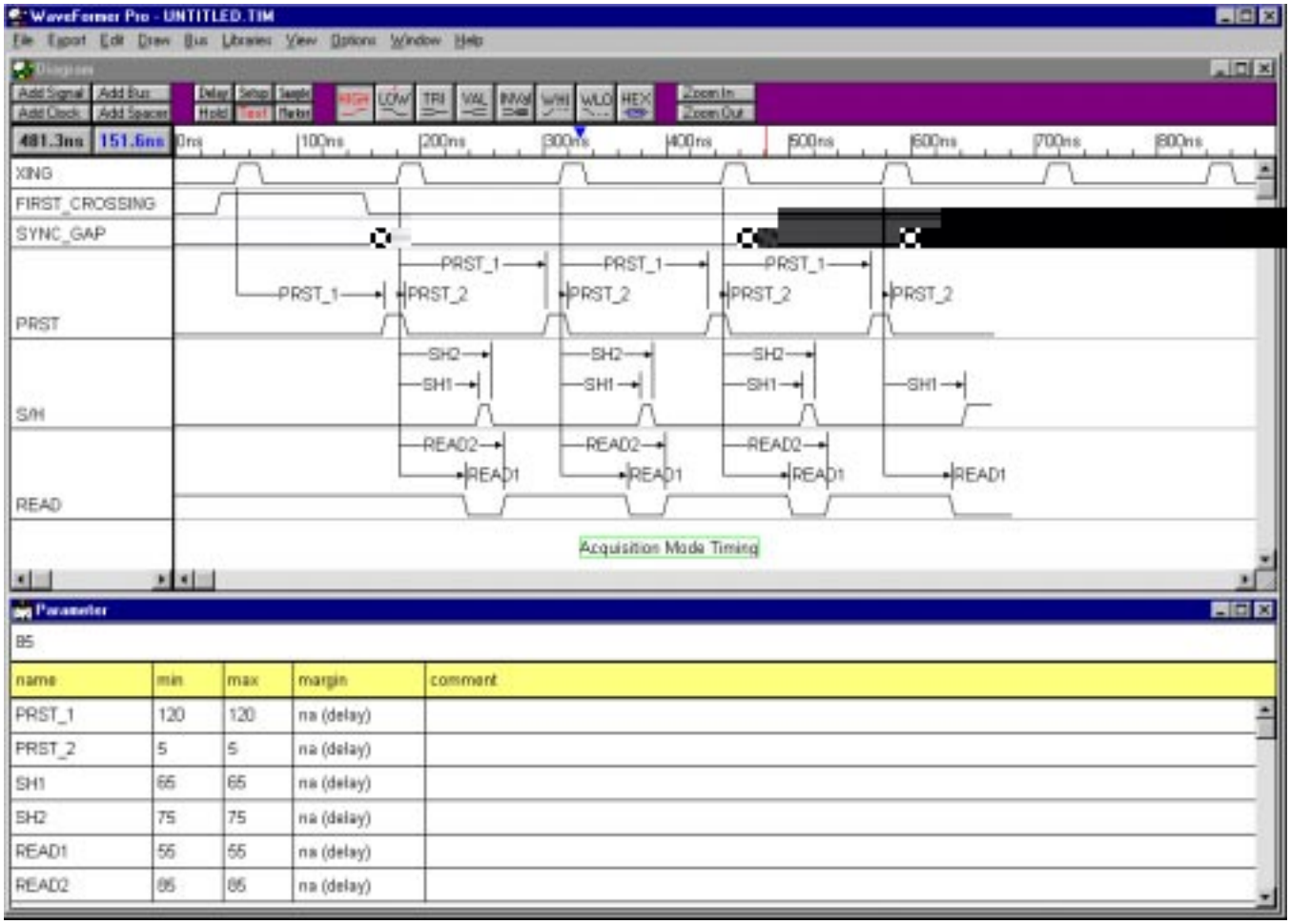
WaveFormer Pro - UNTITLED.TIM
File Export Edit Draw Bus Libraries View Options Window Help
Add Signal
Add Bus
Add Clock
Add Spacer
Delay
Setup
Height
Hold
Reset
Marker
HIGH
LOW
TRI
VAL
INVAL
WHI
WLO
HEX
Zoom In
Zoom Out
481.3ns
151.6ns
0ns
100ns
200ns
300ns
400ns
500ns
600ns
700ns
800ns
XING
FIRST_CROSSING
SYNC_GAP
PRST
SH
READ
PRST_1
PRST_2
SH2
SH1
READ2
READ1
Acquisition Mode Timing
Parameter
B5
name
min
max
margin
comment
PRST_1 120 120 na (delay)
PRST_2 5 5 na (delay)
SH1 65 65 na (delay)
SH2 75 75 na (delay)
READ1 55 55 na (delay)
READ2 85 85 na (delay)

Figure 1

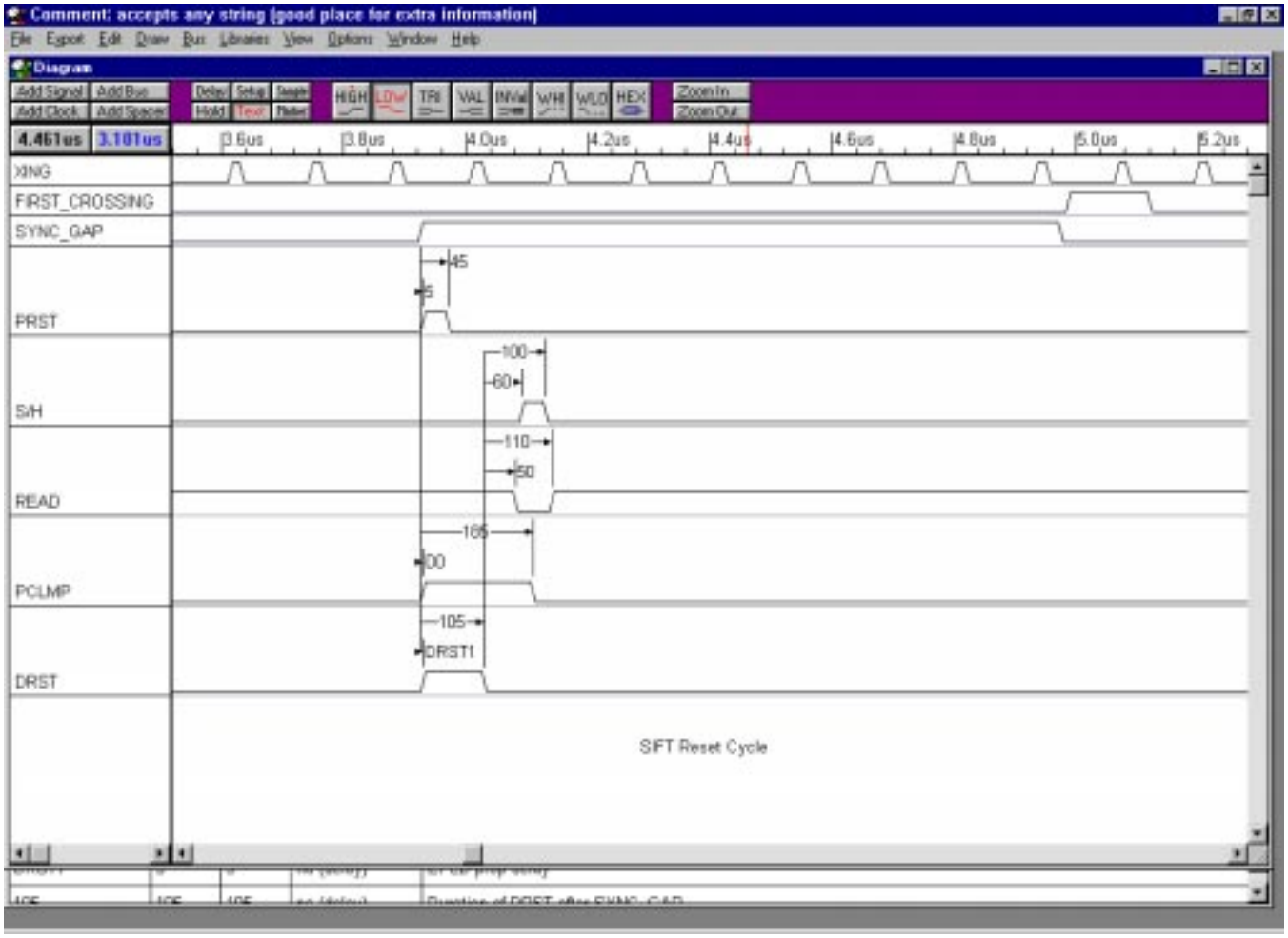

Figure 2

Internal Clock Mode

In Internal mode, a local 53 MHz oscillator runs a small divider that creates a signal essentially the same as XING from the SVX Sequencer. This derived clock is used to run the SIFT/SVX controls as a replacement for the SVX Sequencer XING clock. When in the Internal mode, a counter is used to create the FIRST_CROSSING and SYNC_GAP. The counter increments until 128 XINGs have gone by, and then a Reset Cycle is issued. After the Reset Cycle the counter resets and another 128 Acquisition Cycles are allowed.

Timed Test Outputs

The Clock Generator creates two sets of TREF (Timed REFerence) charge signals. These are enabled by software. If enabled, the TREF signals occur synchronously with a user-selected delay of the XING clock, on the next XING after the VTBG trigger is issued. The variable timing – in 5 nsec steps – allows the user to probe setup and hold times in the SIFT.

Control Link To/From the SVX Sequencer

Two variations of the SVX Sequencer exist, the ‘normal’ and the ‘Standalone’. They differ only in that the ‘Standalone’ requires an input trigger signal from the MCM Test Board and/or the CFT Axial card in order to generate the XING, FIRST_CROSSING and SYNC_GAP signals. This trigger, named SQR_TRIG_OUT on the MCM Test Board, is generated by a write cycle from the on-board microcontroller, typically in response to a 1553 command from the user’s PC. The ‘normal’ SVX Sequencer requires no such interlock, and just drives XING, FIRST_CROSSING and SYNC_GAP all the time.

Control Link To/From the VTBG

The VTBG requires a trigger signal in order to send it's data. The output signal VTBG_TRIG_OUT is generated a programmable number of clock delays from FIRST_CROSSING and continues until the VTBG runs out of data. One data channel from the VTBG is connected to a comparator whose output is monitored by the Clock Generator, allowing the VTBG data to synchronously handshake with the Clock Generator.

Software Viewpoint

The Clock Generator implements three eight-bit registers:

- Event Delay Register, written to by LD_EVENT_DLY
- Clock Control Register, written to by WRT_CLK_CTL
- Clock Status Register, read by asserting CLKCTL_OE*

Event Delay Register

Bit Position(s)	Function on write
7	0: VTBG trigger disabled. 1: VTBG trigger enabled.
6..0	Number of XINGs to delay after FIRST_CROSSING before issuing VTBG trigger, if enabled.

Clock Control Register

Bit Position(s)	Function on write
7	1: Trigger Standalone SVX Sequencer 0: No effect
6	1: Enable TREF0-TREF3 outputs 0: Disable TREF0-TREF3 outputs
5	1: Enable TREF4-TREF6 outputs 0:Disable TREF4-TREF6 outputs
4	1: Force Clock Control to Local Oscillator 0: Allow logic to choose
3..0	Selection code for delay of TREF outputs with respect to XING: 0 XING + 105ns 1 XING + 110 ns 2 XING + 115 ns 3 XING + 120 ns 4 XING + 125 ns 5 XING 6 XING + 5 ns 7 XING + 10 ns 8 XING + 15 ns 9 XING + 20 ns 10 XING + 25 ns 11 XING + 30 ns 12 XING + 40 ns 13 XING + 50 ns 14 XING + 60 ns 15 XING + 70 ns

Clock Status Register

Since the local microcontroller is very slow, no status that changes faster than once every 100 usec is likely to be valid. Therefore, no fast status is included here.

Bit Position(s)	Interpretation on Read
7	1: Clock derived from SVX Sequencer 0: Clock is local
6	1: VTBG Trigger has been issued (cleared by receipt of COMPARATOR input)
5	1: SVX Sequencer Trigger has been issued (cleared by receipt of FIRST_CROSSING)
4	1: TREFs enabled 0: TREFs disabled
3	Status of HDI_EN line
2	Status of COMPARATOR input line
1	Reserved
0	Reserved